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METHOD FOR MODELING INTEGRATED CIRCUIT YIELD

Abstract

A method and system for predicting manufacturing yield for a proposed integrated circuit The method includes: in the order recited: (a) providing a multiplicity of different integrated circuit library elements in a design database, each library element linked to a corresponding normalization factor in the design database; (b) selecting library elements from the design database to include in a proposed design for the integrated circuit; (c) generating an equivalent circuit count of the proposed design based on the normalization factors and a count of each different library element included in the proposed design; and (d) calculating a predicted manufacturing yield based on the equivalent circuit count, a predicted density of manufacturing defects and an area of the proposed integrated circuit chip.